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**PATENT**

**Attorney Docket No.: BEA9-2001-0001-US1**

**BOARD OF PATENT APPEALS**
**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| In re application of: | McKenney | | |
| SERIAL NO.: | 09/816,796 | Group Art Unit: | 2183 |
| FILING DATE: | March 23, 2001 | | |
| FOR: | **A Method of Pipelining Processes In A Multiprocessor** | Examiner: | Tsai, H. |

# BRIEF OF PATENT OWNER ON APPEAL

## 1. *Real Party in Interest*

International Business Machines Corporation, a New York corporation, is the real party in interest.

## 2. *Related Appeals and Interferences*

There are no related appeals or interferences.

## 3. *Status of Claims*

Claims 1-25 remain pending. Claims 1, 12, and 22 were amended in response to the Non-Final Office Action dated February 23, 2005.

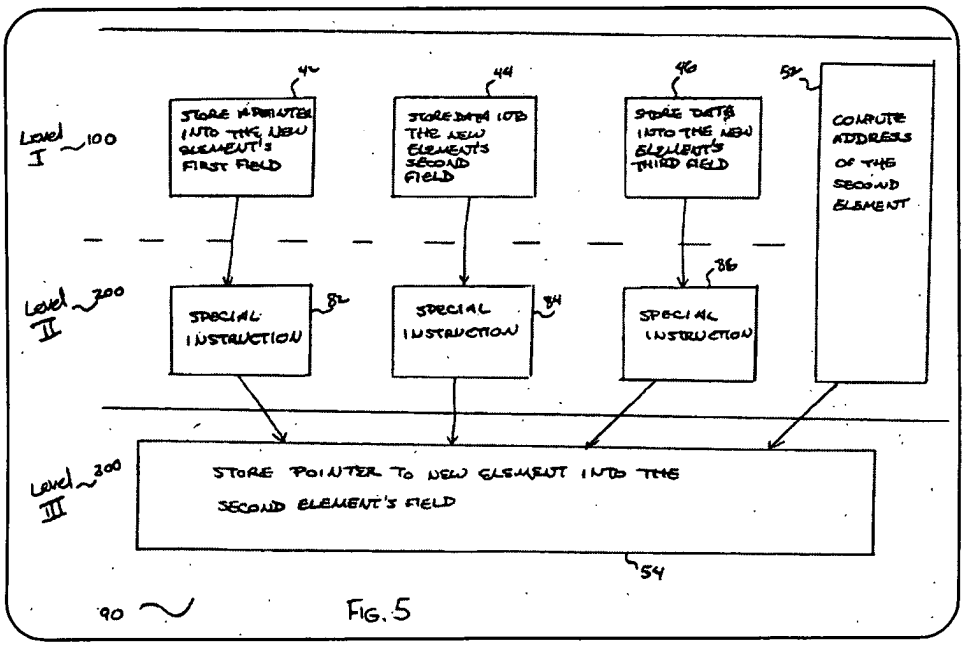
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## 4. *Status of Amendments*

There are no amendments to the claims after final rejection.

## 5. *Summary of Claimed Subject Matter*

Applicant's invention pertains to a computer system having multiple processors and for maximizing performance thereof. Processor performance may be maximized by placing constraints on some classes of memory accesses, while lifting constraints on other classes of memory accesses. Placement and lifting of such constraints removes usage of memory barrier instructions that forces the order of all write operations, and focuses on write operations to memory and so that a CPU may explicitly indicate which write operations are to be specifically ordered, while allowing the remainder of the write operations to occur at any time, *i.e.* it sets the order of write operations with respect to a change in a shared resource. See Applicant's Figure 5, reproduced below.




(Fig. 5 of *McKenney et al.*, US Serial No. 09/816,796)

With respect to claim 1, support for the elements of 1(a) are found in the original

specification on page 8, lines 1-2 and lines 19-20, and page 9, lines 13-14. Support for the elements of 1(b) are found in the original specification on page 8, lines 1-2, lines 4-5, and lines 22-25, and support for elements of 1(c) are found in the original specification on page 8, lines 14-17. In addition, the pseudo code on page 9, lines 1-12 and Fig. 5 show support for each of the elements presented in claim 1.

With respect to claim 12, support for the instructions and ordering of instructions are found in the original specification on page 10, lines 6-13 and supporting pseudo code on page 12, lines 7-15.

With respect to claim 22, support for the instructions and ordering of instructions are found in the original specification on page 10, lines 6-13 and supporting pseudo code on page 12, lines 7-15. In addition support for the "specified state of execution" elements can be found in the original specification on page 10, lines 13-15.

## 6. ***Grounds of Rejection To Be Reviewed On Appeal***

Whether claims 1 and 12 are anticipated by *Robertson*, U.S. Patent No. 5,850,632, under 35 U.S.C. §102(b).

Whether claims 2-6, 13-16, and 23 are anticipated by *Robertson*, U.S. Patent No. 5,850,632, under 35 U.S.C. §102(b).

Whether claims 7-9 and 17-19 and 24 are anticipated by *Robertson*, U.S. Patent No. 5,850,632, under 35 U.S.C. §102(b).

Whether claims 10-11 and 20-21 are anticipated by *Robertson*, U.S. Patent No. 5,850,632, under 35 U.S.C. §102(b).

Whether claim 25 is anticipated by *Robertson*, U.S. Patent No. 5,850,632, under 35

U.S.C. §102(b).

## 7. *Argument*

### A. Rejection of claims 1 and 12 under 35 U.S.C. §102(b).

The Examiner rejected claims 1 and 12 under 35 U.S.C. §102(b) as being anticipated by *Robertson*, U.S. Patent No. 5,850,5632.

In rejecting claims 1 and 12 under 35 U.S.C. §102(b) over *Robertson*, the Examiner is hypothetically applying and equivocating a hardware solution to a software solution. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). The Applicant respectfully submits that claims 1 and 12 would not have been anticipated for the following reasons and a ruling by the Board of Patent Appeals in Applicant's favor and allowance of claims 1 and 12 is respectfully requested.

#### *1. Applicant's Pointer is Not Equivalent to Robertson's Program Counter.*

The Examiner has asserted that program counter register of *Robertson* is equivalent to the pointer claimed by Applicant. "Program counter register in the *Robertson* 632's system, note PC will be incremented or changed to a new number after the write operation." *See Official Action of August 11, 2005, page 3.* Furthermore in the Advisory Action of October 25, 2005, the Examiner states "the value of program counter in the *Robertson* '632's system is interpreted as a pointer since it is the memory address of the next instruction to be fetched during the execution

of a program." As such, the Examiner is asserting that the software based pointer of Applicant is equivalent to a hardware based program counter of a computer processor.

With respect to the pointer element, Applicant claims occurrence of local write operations with respect to storage of a pointer to a new element of a shared resource. It is inherent in both Applicant's invention and *Robertson '632* that a shared resource is stored in non-local memory, since by its very nature a shared item has to be available in a non-local manner so that the objects sharing the item can access the item. To accomplish this, the Examiner asserts that the memory configuration cache of *Robertson '632* is non-local memory. [M]emory configuration cache 305, see Fig. 2, is broadly interpreted as a non-local memory since it is not disposed inside the processors 71-74, see Fig. 2 . . ." See *Office Action of August 11, 2005, page 3.* Accordingly, the Examiner's argument requires that *Robertson* '632 store the value of the program counter in non-local memory in order to equate Applicant's pointer to *Robertson*'s value of the program counter.

However, the memory configuration cache of *Robertson* stores memory configuration information for the memory configuration service unit. The memory configuration service unit of *Robertson* is an ASIC (application specific integrated circuit) which "stores the address range and the memory access parameters for each different memory bank type and for each memory-mapped peripheral type in the particular image system." Col. 9, lines 18-21. There is no program counter in *Robertson's* memory configuration cache, *i.e.* non-local memory adapted to contain a shared resource, because *Robertson's* memory configuration cache stores memory configuration information for the memory configuration service unit, which does not have a program counter. *Robertson's* memory configuration service unit stores address ranges - not a program counter. However, Applicant claims "storing a pointer to a new element of a shared resource." A claim is anticipated only if each and every element as set forth in the claim is

found, either expressly or inherently described in a single prior art reference." MPEP §2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Clearly, *Robertson* does not expressly or inherently describe storing a pointer, or an equivalent thereof, to a new element of a shared resource. Applicant's claimed invention requires the use of the shared resource for storage of the pointer while *Robertson* does not utilize a shared resource for storage of a pointer or even a value of the program counter. Accordingly, Applicant's invention is not anticipated by *Robertson '632*.

### *2. Applicant's Force Element is Not Equivalent to Robertson's Write Element.*

With respect to the force element in Applicant's claims, Applicant requires the force to be associated with storing a pointer to an element of the shared resource. As discussed above, a shared resource is inherently stored in non-local memory, as such storage in non-local memory is required for the resource to be shared. Storing a pointer, or a program counter based upon the Examiner's equivocation, would again require *Robertson* to store the program counter in the memory configuration cache as the shared resource. However, as noted above, *Robertson* cannot store a program counter in the memory configuration cache. Accordingly, *Robertson* does not force a write operation in the manner as claimed by Applicant.

Furthermore, Applicant's claims support that a write operation to non-local memory is forced to occur prior to an action of storing the pointer to a new element of the shared resource. To create an equivalent action in *Robertson*, the Examiner must not only define the memory configuration cache of *Robertson* as non-local memory, but also must define the steps *Robertson* will take based on an event that occurred as a "forced" operation. However, there is no support in *Robertson* for the "force" of the write operations to non-local memory to preceded storing of

the pointer to the new element of the shared resource, even if the non-local memory can be interpreted as memory configuration cache. To reach the Examiner's conclusion, the Examiner assets that the term "force" is a broad term and is "interpreted as the action *Robertson* '632's system will take based on the event occurred." However, there is no force operation associated with the act of storing a pointer to a new element of a shared resource in *Robertson*, either express or inherent, since *Robertson* does not store a program counter in the memory configuration cache. "To establish inherency, the extrinisic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.' " *In re Robertson*, 169 F.3d 743, 49 USPQ 2d 1949 (Fed. Cir. 1999), citing *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991). "The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* As stated above, since *Robertson* does not store a program counter in memory configuration cache, which the Examiner alleges is the equivalent of non-local memory that stores a shared resource, *Robertson* does not inherently teach the "force" element. Accordingly, the Applicant therefor respectfully submits that claims 1 and 12 are not anticipated by *Robertson* ('632) and a ruling by the Board of Patent Appeals in Applicant's favor and allowance of claims 1 and 12 is respectfully requested.

**B. Rejection of claims 2-6, 13-16, and 23 under 35 U.S.C. §102(b).**

The Examiner rejected claims 2-6, 13-16, and 23 under 35 U.S.C. §102(b) as being anticipated by *Robertson*, U.S. Patent No. 5,850,632.

The discussion above regarding *Robertson* is hereby incorporated by reference.

In rejecting claims 2-6, 13-16, and 23 under 35 U.S.C. §102(b) as being anticipated by *Robertson* ('632), the Examiner is alleging that all of the elements in these claims are expressly or inherently taught. Claims 2-6, 13-16, and 23 pertain to use of registers associated with respective instruction addresses to control an order of execution of instructions to support the elements of ordering operations as claimed by Applicant in the respective independent claims. Claims 2-6 are dependent on claim 1, claims 13-16 are dependent on claim 12, and claim 23 is dependent on claim 22. The registers and associated instructions claimed in each of claims 2-6, 13-16, and 23 are for ordering write operations to local and non-local memory, and storage of a pointer to a shared resource, which is inherently stored in non-local memory – otherwise by its very nature it would not be shared. The registers and associated instructions are used to make sure the instructions are executed in a specified order and the pointer to the shared resource is stored in the proper order. As noted above, the Examiner equivocates memory configuration cache of *Robertson* with Applicant's non-local memory and a program counter of *Robertson* with Applicant's pointer. However, also as noted above, *Robertson* cannot and does not store a program counter to an element of a shared resource in the memory configuration cache. "Memory configuration cache service unit 17 responses to memory configuration cycles generated by mulitprocessor integrated circuit 100 . . ." *Robertson*, Col. 9, lines 12-15. Memory configuration cache is a part of the multiprocessor integrated circuit 100. "Memory configuration cache service unit 17 stores the address range and the memory access parameters for each different memory bank type and for each memory-mapped peripheral type in the particular image system." *Robertson*, Col. 9, lines 18-21. As clearly stated in *Robertson*, the memory configuration cache stores memory configuration information in the form of address ranges for the memory configuration service unit. The memory configuration information stores address ranges not a program counter. In fact, a program counter does not appear in the memory configuration cache of *Robertson*. As such, *Robertson* ('632) cannot order instructions to ensure

the program execution and timing of storing the pointer to the shared source. Accordingly, the Applicant therefor respectfully submits that claims 2-6, 13-16, and 23 are not anticipated by *Robertson* ('632) and a ruling by the Board of Patent Appeals in Applicant's favor and allowance of claims 2-6, 13-16, and 23 is respectfully requested.

### C. Rejection of claims 7-9, 17-19, and 24 under 35 U.S.C. §102(b)

The Examiner rejected claims 7-9, 17-19, and 24 under 35 U.S.C. §102(b) as being anticipated by *Robertson*, U.S. Patent No. 5,850,632.

The discussions above regarding *Robertson* is hereby incorporated by reference.

In rejecting claims 7-9, 17-19, and 24 under 35 U.S.C. §102(b) as being anticipated by *Robertson* (632), the Examiner is alleging that all of the elements in these claims are expressly or inherently taught. Claims 7, 17, and 24 pertain to assignment of sequence numbers to instructions to ensure that the instructions are executed in a specified order, and claims 8, 9, 18, and 19 pertain to the manner in which the sequence numbers in the instructions are encoded. Claims 7-9 are dependent on claim 1, claims 17-19 are dependent on claim 12, and claim 24 is dependent on claim 22. The instructions claimed in each of claims 7-9, 17-19, and 24 are for ordering write operations to local and non-local memory, and storage of a pointer to a shared resource, which is inherently stored in non-local memory. The sequence numbers are used to make sure the instructions are executed in a specified order and the pointer to the shared resource is stored in the proper order. As noted above, the Examiner asserts that the memory configuration cache of *Robertson* is equivalent to Applicant's non-local memory and a program counter of *Robertson* is equivalent to Applicant's pointer. However, as noted above, *Robertson*

does not store a program counter to an element of a shared resource in the memory configuration cache. The memory configuration cache of *Robertson* stores address ranges, not a program counter. As such, *Robertson* also cannot order instructions to ensure the program execution and timing of storing the pointer to the shared source. Accordingly, Applicant therefor respectfully submits that claims 7-9, 17-19, and 24 are not anticipated by *Robertson* ('632) and a ruling by the Board of Patent Appeals in Applicant's favor and allowance of claims 1 and 12 is respectfully requested.

### D. Rejection of claim 10-11, 20-21, and 25 under 35 U.S.C. §102(b)

The Examiner rejected claims 10-11, 20-21, and 25 under 35 U.S.C. §102(b) as being anticipated by *Robertson*, U.S. Patent No. 5,850,5632.

The discussions above regarding *Robertson* is hereby incorporated by reference.

In rejecting claims 10-11, 20-21, and 25 under 35 U.S.C. §102(b) as being anticipated by *Robertson* '632, the Examiner is alleging that all of the elements in these claims are expressly or inherently taught therein. Claims 10 and 20 pertain to placement of instructions in a hierarchical order, and claims 11, 21, and 25 include ensuring that the hierarchical order is maintained. The instructions that each of claims 10, 11, 20, 21, and 25 relate includes storage of a pointer to an element of a shared resource, which is inherently stored in non-local memory. The hierarchical ordering of the instructions are used to make sure the instructions are executed in a specified order and the pointer to the shared resource is stored in the proper order. As noted above, the Examiner asserts that the memory configuration cache of *Robertson* is equivalent to Applicant's non-local memory and a program counter of *Robertson* is equivalent to Applicant's pointer.

However, as noted above, *Robertson* does not store a program counter to an element of a shared resource in the memory configuration cache. The memory configuration cache, *i.e.* non-local memory, of *Robertson* stores address ranges, not a program counter. As such, *Robertson* also cannot order instructions to ensure the program execution and timing of storing the pointer to the shared source. Accordingly, the Applicant therefor respectfully submits that claims 10, 11, 20, 21, and 25 are not anticipated by *Robertson* ('632) and a ruling by the Board of Patent Appeals in Applicant's favor and allowance of claims 10, 11, 20, 21, and 25 is respectfully requested.

**E. Rejection of claim 22 under 35 U.S.C. §102(b)**

The Examiner rejected claim 22 under 35 U.S.C. §102(b) as being anticipated by *Robertson*, U.S. Patent No. 5,850,632.

The discussions above regarding *Robertson* is hereby incorporated by reference.

In rejecting claim 22 under 35 U.S.C. §102(b) over *Robertson*, the Examiner is hypothetically applying and equating a hardware solution to a software solution. The Examiner has asserted that a program counter is inherent in *Robertson* and is equivalent to the pointer claimed by Applicant. In addition, the Examiner has asserted that the non-local memory claimed by Applicant is equivalent to the memory configuration cache of *Robertson*. With respect to the pointer element, Applicant claims an instruction to ensure occurrence of local write operations with respect to storage of a pointer to a new element of a shared resource. It is inherent in both Applicant's invention and *Robertson* that a shared resource is stored in non-local memory, as by its very nature an item that is shared has to be available to other systems in a non-local manner. However, the memory configuration cache of *Robertson* ('632) stores memory configuration

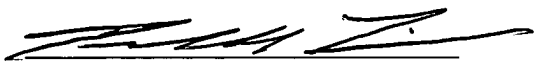
information for the memory configuration service unit, wherein the memory configuration service unit "stores the address range and the memory access parameters for each different memory bank type and for each memory-mapped peripheral type in the particular image system." Col. 9, lines 18-21. There is no program counter in the memory configuration service unit because this service unit stores address ranges – not a program counter. However, Applicant claims the ordering of write operations and "storage of a pointer to a new element of a shared resource." A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." MPEP §2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Clearly, *Robertson* does not expressly or inherently describe storing a pointer, or an equivalent thereof, to a new element of shared resource and storage of the pointer in a shared resource in non-local memory. Therefore, *Robertson* does not provide each and every feature of Applicant's invention as required under 35 U.S.C. §102(b). Accordingly, the Applicant therefor respectfully submits that claim 22 is not anticipated by *Robertson* ('632) and a ruling by the Board of Patent Appeals in Applicant's favor and allowance of claim 22 is respectfully requested.

**F. Conclusion**

In view of the rejections presented by the Examiner, it appears clear that the Examiner is employing a computer hardware reference to assert that each of the elements as claimed by Applicant in Applicant's software solution is either expressly or inherently present therein. Although the prior art cited by the Examiner relates to a shared resource in non-local memory, the reference fails to expressly or inherently teach the elements as presented in Applicant's invention. *Robertson* does not expressly or inherently teach, mention or suggest use of the

pointer in non-local memory, *i.e.* associated with a shared resource. Therefore, Applicant's placement and usage of the pointer associated with the shared resource is not expressly or inherently present in *Robertson,* which is one of the components that is presented in each of Applicant's independent claims, *i.e.* storage of a pointer to a new element in a shared resource. Accordingly, Applicant submits that each of the pending claims is not anticipated by *Robertson* and a ruling by the Board of Patent Appeals in Applicant's favor and allowance of the pending claims is respectfully requested.

Respectfully submitted,

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Date: January 17, 2006

## *8. Claims Appendix:*

1. A method for maximizing CPU performance in a multiprocessor, comprising:

allowing write operations in local memory to execute in an arbitrary order and at any time prior to storing a pointer to a new element of a shared resource;

explicitly indicating a set of write operations to non-local memory be conducted in a specified order; and

forcing said write operations to non-local memory to precede storing said pointer to said new element of said shared resource.

2. The method of claim 1, further comprising assigning first and second registers of a CPU for storing associated first and second instruction addresses.

3. The method of claim 2, further comprising providing a third instruction referencing said registers.

4. The method of claim 3, wherein said third instruction specifies ordering between said first and second instructions.

5. The method of claim 4, wherein said third instruction indicates said first instruction's execution attaining a first specified state of execution prior to said second instruction's execution attaining a second specified state of execution.

6. The method of claim 5, wherein said first and said second specified states of execution are selected from the group consisting of: committing instruction execution, initiating memory access, completing a memory access, initiating an I/O access, completing an I/O access, and completing instruction execution.

7. The method of claim 1, further comprising assigning a sequence number to an associated instruction for maintaining instruction ordering.

8. The method of claim 7, further comprising statically encoding said sequence number within said instruction.

9. The method of claim 7, further comprising dynamically encoding said sequence number within said instruction.

10. The method of claim 1, further comprising placing a range of instructions into a hierarchical ordering system.

11. The method of claim 10, further comprising implementing a special instruction for maintaining a hierarchical execution of said instruction.

12. A processor for use in a multiprocessor computer system, comprising:

a first instruction for allowing write operations in local memory to occur in an

arbitrary order; and

a second instruction for explicitly indicating a set of write operations to non-local memory to be conducted in a specified order; and

a special instruction to force execution of said write operations to non-local memory to precede storage of a pointer to a new element of a shared resource.

13. The processor of claim 12, further comprising a first register to store a first instruction address and a second register to store a second instruction address.

14. The processor of claim 13, further comprising a third instruction to manage order of execution of said first and second instructions.

15. The processor of claim 14, wherein execution of said second instruction is responsive to said first instruction reaching a specified state of execution.

16. The processor of claim 15, wherein said specified state of execution is selected from the group consisting of: committing instruction execution, initiating memory access, completing a memory access, initiating an I/O access, completing an I/O access, and completing instruction execution.

17. The processor of claim 12, wherein said first and second instructions are assigned a sequence number to specify an order of instruction execution.

18. The processor of claim 17, wherein said sequence number is statically encoded within said instruction.

19. The processor of claim 17, wherein said sequence number is dynamically encoded within said instruction.

20. The processor of claim 12, further comprising a manager to place a range of instructions in a hierarchical order.

21. The processor of claim 19, further comprising a special instruction to maintain execution of said instruction in said hierarchical order.

22. A processor for use in a multiprocessor computer system, comprising:

a first instruction for allowing write operations in local memory to occur in an arbitrary order;

a second instruction for explicitly indicating a set of write operations to non-local memory to be conducted in a specified order, wherein write operations to non-local memory must execute prior to storage of a pointer to a new element of a shared resource; and

a third instruction for managing order of execution of said first and second instructions;

wherein execution of said second instruction is responsive to said first instruction

reaching a specified state of execution and said specified state of execution is selected from the group consisting of: committing instruction execution, initiating memory access, completing a memory access, initiating an I/O access, completing an I/O access, and completing instruction execution.

23. The processor of claim 22, a first register to store a first instruction address and a second register to store a second instruction address.

24. The processor of claim 22, wherein said first and second instructions are assigned a sequence number to specify an order of instruction execution.

25. The processor of claim 22, further comprising a special instruction to maintain execution of said instructions in said hierarchical order.

## 9. *Evidence Appendix*

U.S. Patent Application No. 5,850,632 to Robertson

In re Robertson, 169 F.3d 743, 49 USPQ 2d 1949 (Fed. Cir. 1999)

MPEP §2131

## *10. Related Proceedings Appendix*

None

Westlaw.

169 F.3d 743

Page 1

169 F.3d 743, 49 U.S.P.Q.2d 1949
**(Cite as: 169 F.3d 743)**

**C**
Briefs and Other Related Documents

United States Court of Appeals,Federal Circuit.
In re Anthony J. ROBERTSON and Charles L. Scripps.
**No. 98-1270.**

Feb. 25, 1999.

Applicant sought patent for fastening and disposal system for diapers. The Board of Patent Appeals and Interferences rejected application as anticipated and obvious in light of prior art, and applicant appealed. The Court of Appeals, Friedman, Senior Circuit Judge, held that proposed claim was not inherent in prior art reference and thus was not anticipated by that reference.

Reversed.

Rader, Circuit Judge, filed concurring opinion.

West Headnotes

[1] **Patents 291 ⚿72(1)**

291 Patents
291II Patentability
291II(D) Anticipation
291k72 Identity of Invention
291k72(1) k. In General. Most Cited Cases
Anticipation of patent claim requires that each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. 35 U.S.C.A. § 102(e).

[2] **Patents 291 ⚿66(1.11)**

291 Patents
291II Patentability
291II(D) Anticipation
291k63 Prior Patents
291k66 Operation and Effect
291k66(1.11) k. Clothing and Fabrics. Most Cited Cases
Proposed patent claim for fastening and disposal system for diapers, which recited third mechanical fastening means, separate from fastening means to attach diaper to wearer, to secure diaper for disposal was not inherent in prior art patent that did not expressly include third fastening means for disposal, but suggested only that diaper could be closed by using same fastening means used for initially attaching diaper to body, and proposed claim thus was not anticipated by prior art patent. 35 U.S.C.A. § 102(e).

[3] **Patents 291 ⚿65**

291 Patents
291II Patentability
291II(D) Anticipation
291k63 Prior Patents
291k65 k. Sufficiency of Description. Most Cited Cases
If prior art reference does not expressly set forth particular element of patent claim, that reference still may anticipate claim if that element is inherent in its disclosure. 35 U.S.C.A. § 102(e).

[4] **Patents 291 ⚿65**

291 Patents
291II Patentability
291II(D) Anticipation
291k63 Prior Patents
291k65 k. Sufficiency of Description. Most Cited Cases
To establish that particular element of patent claim is inherent in prior art reference, for purpose of finding anticipation, extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill; inherency, however, may not be established by probabilities or possibilities,

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and mere fact that a certain thing may result from a given set of circumstances is not sufficient. 35 U.S.C.A. § 102(e).

[5] **Patents 291 ⇐324.2**

291 Patents
291XII Infringement
291XII(C) Suits in Equity
291k324 Appeal
291k324.2 k. Decisions Reviewable. Most Cited Cases
Court of Appeals would not consider theory propounded by patent commissioner, in appellate brief, for upholding rejection of patent claim on grounds of obviousness, where such theory was not the ground on which the Board of Patent Appeals and Interferences based its obviousness ruling.

***744** Kenneth R. Adamo,Jones, Day, Reavis & Pogue, of Cleveland, Ohio, argued for appellant. With him on the brief were Calvin P. Griffith, and Gregory A. Castanias, of Washington, DC. Of counsel on the brief was Steven W. Miller, The Proctor & Gamble Company, of Cincinnati, Ohio.
Linda Moncys Isacson, Associate Solicitor, Office of the Solicitor, of Arlington, Virginia, argued for appellee. With her on the brief were Albin F. Drost, Acting Solicitor, and John M. Whealan, Associate Solicitor.

Before NEWMAN, Circuit Judge, FRIEDMAN, Senior Circuit Judge, and RADER, Circuit Judge.

Opinion for the court filed by Senior Circuit Judge FRIEDMAN, in which Circuit Judge PAULINE NEWMAN joins. Concurring opinion filed by Circuit Judge RADER.
FRIEDMAN, Senior Circuit Judge:
This appeal challenges the decision of the Board of Patent Appeals and Interferences (Board) that claim 76 in the appellants' patent application was anticipated by and obvious over United States Patent No. 4,895,569 (the Wilson patent). We reverse.

I

Both claim 76 and Wilson involve fastening and disposal systems for diapers. In both, the body of the diaper features a small front and a larger rear section. The outer edges of those sections are attached at the wearer's waist in the hip area. Once the diaper is soiled and then removed, the smaller front section is rolled up into the larger rear section and secured in this rolled-up configuration by fasteners.

The appellants' application is for "an improved mechanical fastening system for ... disposable absorbent articles [*i.e.*, diapers] that provides convenient disposal of the absorbent article." Claim 76 covers:
[A] mechanical fastening system for forming side closures ... comprising
a closure member ... comprising a first mechanical fastening means for forming a closure, said first mechanical fastening means comprising a first fastening element;
a landing member ... comprising a second mechanical fastening means for forming a closure with said first mechanical fastening means, said second mechanical fastening means comprising a second fastening element mechanically engageable with said first element; and
disposal means for allowing the absorbent article to be secured in a disposal configuration after use, said disposal means comprising a third mechanical fastening means for securing the absorbent article in the disposal configuration, said third mechanical fastening means comprising a third fastening element mechanically engageable with said first fastening element ...

Claim 76 thus provides for two mechanical fastening means to attach the diaper to the wearer and a third such means for securing the diaper for disposal.

The Wilson patent discloses two snap elements on fastening strips attached to the outer edges of the front and rear hip sections of the garment. The fastening strips may also include "secondary load-bearing closure means"-additional fasteners to secure the garment; they may be identical to the snaps.

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Wilson also states:
[D]isposal of the soiled garment upon removal from the body is easily accomplished by folding the front panel ... inwardly and then fastening the rear pair of mating fastener members ... to one another, thus neatly bundling the garment into a closed compact package for disposal.

*745 In other words, Wilson does not provide a separate fastening means to be used in disposing of the diaper. Instead, it suggests that disposal of the used diaper may be "easily accomplished" by rolling it up and employing the same fasteners used to attach the diaper to the wearer to form "a closed compact package for disposal."

In holding that the invention claim 76 covers was anticipated by Wilson, the Board did not hold that Wilson set forth a third fastening means. Instead, it found that Wilson anticipated claim 76 "under principles of inherency." Applying the language of claim 76 to the operation of Wilson, it concluded that "an artisan would readily understand the disposable absorbent garment of Wilson ... as being inherently capable of [making the secondary load-bearing closure means] (third fastening element) mechanically engageable with [the other snap fasteners on the fastening strip] (first fastening element)"-*i.e.*, using the secondary closure not with its mate, but with one of the primary snap fasteners. The Board summarily affirmed the examiner's alternative ruling that claim 76 would have been obvious in light of Wilson because "claim 76 lacks novelty."

II

[1] Anticipation under 35 U.S.C. § 102(e) requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed.Cir.1987).

[2] A. The Wilson patent does not expressly include a third fastening means for disposal of the diaper, as claim 76 requires. That means is separate from and in addition to the other mechanical fastening means and performs a different function than they do. Indeed, Wilson merely suggests that the diaper may be closed for disposal by using the same fastening means that are used for initially attaching the diaper to the body.

[3] [4] If the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if that element is " inherent" in its disclosure. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. " *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed.Cir.1991). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* at 1269, 948 F.2d 1264, 20 U.S.P.Q.2d at 1749 (quoting *In re Oelrich*, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A.1981)).

In finding anticipation by inherency, the Board ignored the foregoing critical principles. The Board made no attempt to show that the fastening mechanisms of Wilson that were used to attach the diaper to the wearer also "necessarily" disclosed the third separate fastening mechanism of claim 76 used to close the diaper for disposal, or that an artisan of ordinary skill would so recognize. It cited no extrinsic evidence so indicating.

Instead, the Board ruled that one of the fastening means for attaching the diaper to the wearer also could operate as a third fastening means to close the diaper for disposal and that Wilson therefore inherently contained all the elements of claim 76.
In doing so, the Board failed to recognize that the third mechanical fastening means in claim 76, used to secure the diaper for disposal, was separate from and independent of the two other mechanical means used to attach the diaper to the person. The Board's theory that these two fastening devices in Wilson were capable of being intermingled to perform the same function as the third and first fastening elements in claim 76 is insufficient to

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show that the latter device was inherent in Wilson. Indeed, the Board's analysis rests upon the very kind of probability or possibility-the odd use of fasteners with other than their mates-that this court has pointed out is insufficient to establish inherency.

III

The Board's entire discussion of obviousness was as follows:
***746 *The rejection of claim 76 under 35 USC § 103***
We sustain the rejection of claim 76 under 35 USC § 103.
Above, we found that claim 76 lacks novelty. Lack of novelty is the ultimate of obviousness. See *In re Fracalossi,* 681 F.2d 792, 794, 215 USPQ 569, 571 (CCPA 1982). Thus, claim 76 is appropriately rejected under 35 USC § 103 as being unpatentable.

The "lack of novelty" upon which the Board based its conclusion of obviousness, however, was its finding of anticipation. Our rejection of that finding eliminates the sole basis of the Board's obviousness determination, which therefore cannot stand. *See In re Adams,* 53 C.C.P.A. 1433, 364 F.2d 473, 480, 150 U.S.P.Q. 646, 651 (1966).

In his brief the Commissioner argues:
Moreover, even if this court interprets claim 76 to require two separate fasteners to perform the closure and disposal functions, it would have been well within the knowledge of one of ordinary skill in the art to take Wilson's one fastener and make it into two separate fasteners. *See* [*In re* ] *Graves,* 69 F.3d [1147,] 1152, 36 USPQ2d [1697,] 1701 [ (Fed.Cir.1995) ] (When evaluating a reference, it is appropriate to consider the knowledge of a skilled artisan in combination with the teaching of the reference.). Accordingly, claim 76 would have been obvious to one of ordinary skill in the art, and the rejection should be affirmed by this Court.

[5] That, of course, was not the ground on which the Board based its obviousness ruling. We decline to consider counsel's newly-minted theory as an alternative ground for upholding the agency's decision. *See In re Soni,* 54 F.3d 746, 751, 34 U.S.P.Q.2d 1684, 1688 (Fed.Cir.1995) (citing *In re DeBlauwe,* 736 F.2d 699, 705 n. 7, 222 U.S.P.Q. 191, 196 n. 7 (Fed.Cir.1984)). The Board's obviousness ruling cannot be sustained on the ground the Board gave.

CONCLUSION

The decision of the Board of Patent Appeals and Interferences affirming the examiner's rejection of claim 76 as anticipated by and obvious over the Wilson patent is

*REVERSED.*

RADER, Circuit Judge, concurring.
Robertson asserts that the prior art Wilson patent does not teach three elements of claim 76: a "third mechanical fastening means," a disposal means on the "outside surface" of the body portion, and end regions that are "in an overlapping configuration when worn." In reversing the Board, this court relies solely on the purported failure of Wilson to teach the third fastening means. Because I believe Wilson teaches such a means, but does not teach the other two limitations at issue, I concur.

In its analysis, this court assumes without discussion that the claimed "third mechanical fastening means" covers a *separate* third mechanical fastening means. This issue is key, for if the claim does not require a separate third fastening means, but instead allows the first fastening means to also serve as the third, then the prior art Wilson patent clearly teaches that element of the claim. For two reasons, this claim does not, to my eyes, require a separate third fastening means. First, the claim does not specifically recite a *separate* third fastening means. Second, because the claim is in means-plus-function form, this court consults the specification to identify structure. The specification explicitly teaches that the first and third fastening elements can be the same so long as they are complementary, as they are in Wilson. Accordingly, I agree with the Board that Wilson teaches the claimed "third fastening element."

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Wilson does not, however, teach either of the other two claim limitations at issue. As to the disposal means on the "outside surface" of the body portion, Wilson's figs. 12 and 13a-d show the disposal means on the inside of the body portion. As to the end regions that are "in an overlapping configuration when worn," Wilson explicitly teaches that the end regions should abut, not overlap, when worn. To overcome these teachings, the Board relied on the following statement in Wilson: "Further, the fastener members ***747** need not be previously mounted on a separate strip as shown then bonded ... to the stretchable outer cover.. .. Multi-component snaps are available which may be applied directly to a stretchable outer cover material...." Col. 7, l. 65 to col. 8, l. 3. The Board opined that applying snaps directly to the outer cover would result in both a disposal means on the " outside surface" and end regions "in an overlapping configuration when worn." Simply put, the Board has put more weight on this teaching than it can bear. It is far from clear what effect applying the snaps directly to the outer cover will have on the Wilson diaper configuration, let alone that it will result in a configuration satisfying the claim elements at issue. Accordingly, because I believe that the Board clearly erred in this interpretation of Wilson, I would reverse on this ground.

C.A.Fed.,1999.
In re Robertson
169 F.3d 743, 49 U.S.P.Q.2d 1949

Briefs and Other Related Documents (Back to top)

- 1998 WL 34099956 (Appellate Brief) Reply Brief for Appellants (Aug. 14, 1998) Original Image of this Document (PDF)
- 1998 WL 34099954 (Appellate Brief) Brief for Appellee Commissioner of Patents and Trademarks (Jul. 14, 1998) Original Image of this Document with Appendix (PDF)
- 1998 WL 34099953 (Appellate Brief) Corrected Brief for Appellants (May. 18, 1998) Original Image of this Document with Appendix (PDF)
- 98-1270 (Docket) (Mar. 02, 1998)

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# 2131 Anticipation - Application of - 2100 Patentability

## 2131 Anticipation - Application of 35 U.S.C. 102(a), (b), and (e) [R-1]

### 35 U.S.C. 102 Conditions for patentability; novelty and loss of right to patent.

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent, or

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States, or

(c) he has abandoned the invention, or

(d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor"s certificate filed more than twelve months before the filing of the application in the United States, or

**>

(e) the invention was described in - (1) an application for patent, published under **section 122(b)**, by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in **section 351(a)** shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under **Article 21(2)** of such treaty in the English language; or<

(f) he did not himself invent the subject matter sought to be patented, or

(g)(1) during the course of an interference conducted under **section 135** or **section**

**291**, another inventor involved therein establishes, to the extent permitted in **section 104**, that before such person's invention thereof the invention was made by such other inventor and not abandoned, suppressed, or concealed, or (2) before such person's invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under this subsection, there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

---

**TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM**

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). >"When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art." *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) (claim to a system for setting a computer clock to an offset time to address the Year 2000 (Y2K) problem, applicable to records with year date data in "at least one of two-digit, three-digit, or four-digit" representations, was held anticipated by a system that offsets year dates in only two-digit formats). See also MPEP § **2131.02**.< "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Note that, in some circumstances, it is permissible to use multiple references in a **35 U.S.C. 102** rejection. See **MPEP § 2131.01**.

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**Attorney Docket No.: BEA9-2001-0001-US1**

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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|---|---|---|---|
| In re application of: | McKenney | | |
| SERIAL NO.: | 09/816,796 | Group Art Unit: | 2183 |
| FILING DATE: | March 23, 2001 | | |
| FOR: | **A Method of Pipelining Processes In A Multiprocessor** | Examiner: | Tsai, H. |

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Enclosed is a Brief in Support of Appeal with copies of all references which were relied upon by Appellant, and a Credit Card Payment Form in the amount of $500.00 pursuant to 37 C.F.R. §1.17(c).

Respectfully submitted,

By: _____
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